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| 09/048,932 | 03/26/1998 | DEAN A. KLEIN | MEI-97-01386 | 4878 |

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PARK, VAUGHAN & FLEMING LLP
508 SECOND STREET
SUITE 201
DAVIS, CA 95616

| EXAMINER |
|---|
| LO, LINUS H |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2614 | |

DATE MAILED: 11/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

HG

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/048,932 | KLEIN, DEAN A. | |
| | Examiner | Art Unit | |
| | Linus H Lo | 2614 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 August 2002, Amendment* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,9-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. It is noted that the instant application does not explicitly describe "the north bridge" in any specific definition or description , thus it is considered for art rejection purpose, the claimed " north bridge chip" is interpreted as "a logic chip" that has the equivalent function as the described core logic unit on page 5, lines 12-13

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7, 10, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208 (of record) in view of So '559(New).

Considering claim 1(Thrice Amended), Dea discloses a device relating to the field of video processing and in particular, to the compression and decompression of video signals. Dea discloses the following subject matter, note:

a) the claimed video input port, for receiving video data for a current video frame is met by bus interface 200 ( FIG. 2, column 6, lines 42-44);

b) the claimed video input buffer coupled to the video input port , for storing video data from the video input port is met by the current frame memory 204 ( FIG. 2, 3A, and column 6, lines 42-44) ;

c) the claimed previous frame buffer , for storing at least a portion of a previous video frame is met by previous image memory 206 ( FIG. 2, 3A and column 5, lines 38-47), wherein the described previous image block is the previous video frame;

d) the claimed operation unit coupled to the video input buffer and the previous frame buffer, for performing an operation between data from the video input buffer and data from the previous frame buffer is met by the compression/decompression accelerator 120 ( FIG. 2, 3A , and column 9, line 57- column 10, line 3), whereas the described frame difference determination by the frame difference block 220 is considered as the claimed operation;

e) the claimed result buffer coupled to the operation unit , for storing the result of an operation from the operation unit is met by the encoded data storage buffer 248(332) ( FIG. 2, 3A, and column 9, line 57- column 10, line 3, column 15, lines 8-13 and column 10, line 53-column 11, line 7); and

f) the limitation of wherein the apparatus *reside as a core logic circuit* for a computer system as described by the compress/decompression accelerator 120 that includes the function frame difference block 220 ( column 6, lines 36-44, and column 5, lines 42-47, and FIG. 1 and 2), where the description at column 5 and Fig. 2 elucidated the compressor/decompressor 120 is a circuitry within the video interface system that interface with the processor 112 to the RAM by way of accelerator bus interface.

However Dea does not explicitly disclose the claimed **apparatus resides insides of a north bridge core logic chip** for a computer system so that the signal are provided with a higher bandwidth pathway to improve throughput.

Nonetheless Dea teaches the comprssion/depression accelerator 120 as a core logic unit for a computer system as described above at (f).

So discloses an integrated circuit provides on a single chip for use with a first processor off-chip. So discloses that a VSP (wrapper-and-digital signal processor-core) used as a **graphic accelerator** that is provided either as the North bridge or AGP graphic/video chip as described at column 17, lines 24-43, in which the data after the VSP processing, the data will then be passed out with higher bandwidth. It is noted that So also discloses that accelerator (core logic unit) is provided at the North Bridge chip, and whereas such implementation which has the advantage of achieving MIPS (millions of instructions per second) column 4, lines 14-16, without substantially loading PCI , peripheral component interface bus (column 17, lines 24-32).

Therefore the examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dea's teaching of video accelerator (core logic unit ) with the teaching of **graphic accelerator** that is provided either at the **North bridge chip** for the stated advantage.

Considering claim 2, the claimed memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a memory that stores video data from

the video input port and result data from the result buffer is met by bus interface 200 (FIG. 2, column 5, lines 38-47, and column 7, lines 39-44), in which the passage from column 5 described that the memory port is coupled to the previous frame buffer, while excerpt from column 7 described the memory port is coupled to the result buffer.

Considering claim 3, the system of Dea and So discloses all the claimed limitations except for the claimed memory **coupled to the memory port** for storing the video data form the video input port and result data from the result buffer, wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory.

Nonetheless, Dea discloses *a memory for storing the video data form the video input port and result data from the result buffer,* wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory 114 (column 10, lines 39-46, and column 11, lines 8-18), in which the excerpt from column 10 discloses that the video data is stored in a current frame area in the memory 114, and the passage from column 11 discloses the result data is stored in a difference frame area in the memory 114. As such, a memory port inherently exists with respect to the memory 114 to facilitate the transfer of data to and from the compression /decompression accelerator 120.

Considering claim 4, the claimed wherein the memory stores a current video frame and a previous video frame in the same location in the memory, allowing the current video

frame to be written over the previous video frame is met by the description at column 12, lines 24-44, whereas the described physical buffer memory 350 which originally stores previous image and subsequently a current image is being stored in the same location in physical buffer memory 350.

Considering claim 5, the system of Dea and So discloses the claimed invention except for the claimed wherein the memory also stores instructions and data for a central processing unit of a computer system.

Dea teaches *a memory* for the computer system in the memory as the description of DRAM 114 at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Examiner takes Official Notice that it is both notoriously well-known in the art to integrate video processing systems in computer systems, and to consolidate storage for disparate processes in common memories.

Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the Dea and So accordingly in order to provide a computer backbone to facilitate the video processing, and to make efficient use of memory storage capacity.

Considering claim 7, note:

a) the claimed video input buffer stores a block of data from the video input port is met by the data of current image block 326 ( column 6, lines 42-44 and column 10, lines 53-56);

b) the claimed previous frame buffer stores a block of data from the previous video frame is met by previous image block (column 5, lines 38-47);

c) the claimed result buffer stores a block of data from the operation unit is met by the buffer 248 (column 10, lines 53-56, and column 9, line 60- column 10, line 3); and

d) the claimed operation unit performs an operation between a block of data from the video input port and a block of data from the previous frame buffer is met by the description at column 9, line 60- column 10, line 3, where the frame different block 220 is considered as the operation unit.

Considering claim 10, the claimed additional resources within the apparatus, for compressing the video data from the video input port is met by the element in FIG. 2 and description at column 6, lines 36-64, where the compression/decompression accelerator 120 consists of additional resources for the purpose of compression.

Considering claim 20(Thrice amended), claim 20 recites the same limitations as in claim 1, namely the claimed video input port, the video input buffer, the previous frame buffer, the operation unit and the result buffer and the apparatus as a core logic chip, thus claim 20 is rejected for the same reason as claim 1 above. Additionally, the claimed central processing

unit within the computer system is met by the processor 112 ( FIG. 1 and column 4, lines 37-45).

Considering claim 12, the system of Dea and So discloses all the claimed limitation except for the claimed video input buffer being a register that **stores less than one video frame**.

However, smaller storage capacity memory devices have the benefit of more cost efficiency in manufacturing.

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dea and So teachings accordingly for the stated advantage.

4. Claims 6, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea and So and further in view of Abramatic et al. '383 (of record) .

Considering claim 6, the system of Dea and So discloses the claimed invention except for the claimed limitation of wherein the operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer.

Nonetheless, Dea teaches that the operation unit performs *a computing of the difference frame* between data from the video input buffer and data from the previous frame buffer as discuss above in claim 1.

Additionally, Abramatic et al. teach that a form of compression consists detecting variations (difference) between one image and the next image as described at column 2, lines

53-56. Abramatic et al. discloses the claimed operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Abramatic et al. teaches that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidated at column 7, lines 32-35. Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to modify the Dea and So combination with such teaching for the stated advantage.

Considering claim 13(Thrice Amended), Dea discloses a device relating to the field of video processing and in particular, to the compression and decompression of video signals. Dea discloses the following claimed subject matter, note :

a) the claimed video input port, for receiving video data for a current video frame is met by bus interface 200 ( FIG. 2, column 6, lines 42-44);

b) the claimed video input buffer coupled to the video input port , for storing video data from the video input port is met by the current frame memory 204 ( FIG. 2, 3A, and column 6, lines 42-44) ;

c) the claimed previous frame buffer , for storing at least a portion of a previous video frame is met by previous image memory 206 ( FIG. 2, 3A and column 5, lines 38-47), wherein the described previous image block is the previous video frame;

d) the claimed result buffer coupled to the operation unit , for storing the result of an operation from the operation unit is met by the encoded data storage buffer 248(332) ( FIG. 2, 3A, and column 9, line 57- column 10, line 3, column 15, lines 8-13 and column 10, line 53-column 11, line 7); and

e) the claimed memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a memory that stores video data from the video input port and result data from the result buffer is met by bus interface 200 (FIG. 2, column 5, lines 38-47, and column 7, lines 39-44), wherein the passage from column 5 described that memory port coupled to previous frame buffer, while excerpt from column 7 described the memory port coupled to result buffer.

However, Dea does not explicitly disclose the following limitations , note:

i) the claimed exclusive-OR unit coupled to the video input buffer and the previous frame buffer, for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer, and

ii) the claimed memory coupled to the memory port for storing the video data from the video input port and result data from the result buffer, wherein the video data is stored in a current frame in the memory and the result data is stored in a difference frame in the memory.

iii) the claimed wherein the apparatus resides inside of a north bridge chip for a computer system so that graphic signals are provided with a higher bandwidth pathway to improve throughput.

In regarding to (i), Dea teaches that *an operation unit* coupled to the video input buffer and the previous frame for performing *a computing of the difference frame* between data from the video input buffer and data from the previous frame buffer as described by the compression/decompression accelerator 120 ( FIG. 2, 3A , and column 9, line 57- column 10, line 3), wherein the described frame difference determination by the frame difference block 220 is considered as the operation.

Nonetheless, Abramatic et al. teaches that a form of compression consists in detecting variations (difference) between one image and the next image as described at column 2, lines 53-56. Abramatic et al. discloses the claimed exclusive-OR unit , for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer as met by the description at column 6, lines 52-58, in which the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Since Abramatic et al. teach that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidated at column 7, lines 32-35. Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to modify the system of Dea with such teachings for the stated advantage.

In regarding to (ii), Dea discloses *a memory for storing the video data form the video input port and result data from the result buffer,* wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory 114 (column 10, lines 39-46, and column 11, lines 8-18), in which the excerpt from

column 10 discloses that the video data is stored in a current frame area in the memory 114, and the passage from column 11 discloses that the result data is stored in a difference frame area in the memory 114. As such, a memory port inherently exists with respect to the memory 114 to facilitate the transfer of data to and from the compression /decompression accelerator 120.

In regarding (iii) , Dea teaches the apparatus *reside as a core logic circuit* for a computer system as described by the compress/decompression accelerator 120 that includes the function frame difference block 220 ( column 6, lines 36-44, and column 5, lines 42-47, and FIG. 1 and 2), where the description at column 5 and Fig. 2 elucidates the compressor/decompressor 120 is a circuitry within the video interface system that interfaces with the processor 112 to the RAM by way of accelerator bus interface.

So discloses an integrated circuit provides on a single chip for use with a first processor off-chip. So discloses that a VSP (wrapper-and-digital signal processor-core) used as a **graphic accelerator** that is provided either as the North bridge or AGP graphic/video chip as described at column 17, lines 24-43, in which the data after the VSP processing, the data will then be passed out with higher bandwidth. It is noted that So also discloses that accelerator (core logic unit) is provided at the North Bridge chip, and whereas such implementation which has the advantage of achieving MIPS (millions of instructions per second) column 4, lines 14-16, without substantially loading PCI , peripheral component interface bus (column 17, lines 24-32).

Therefore the examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dea's teaching of video

accelerator (core logic unit ) with the teaching of **graphic accelerator** that is provided either at the **North bridge chip** for the stated advantage.

Considering claim 14, the claimed wherein the memory stores a current video frame and a previous video frame in the same location in the memory, allowing the current video frame to be written over the previous video frame is met by the description at column 12, lines 24-44, whereas the described physical buffer memory 350 which originally stores previous image and subsequently a current image is being stored in the same location in physical buffer memory 350.

Considering claim 15, the system of Dea, So and Abramatic et al. discloses all the claimed limitations except for the claimed limitation wherein the memory also stores instructions and data for a central processing unit of a computer system.

Dea teaches *a memory* for the computer system in the memory as the description of DRAM 114 at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Examiner takes Official Notice that it is both notoriously well-known in the art to integrate video processing systems in computer systems, and to consolidate storage for disparate processes in common memories.

Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the system of Dea, So and Abramatic et al. accordingly in order to provide a computer backbone to facilitate the video processing, and to make efficient use of memory storage capacity.

Considering claim 16, note:

a) the claimed video input buffer stores a block of data from the video input port is met by the data of current image block 326 of Dea ( column 6, lines 42-44 and column 10, lines 53-56);

b) the claimed previous frame buffer stores a block of data from the previous video frame is met by previous image block of Dea (column 5, lines 38-47);

c) the claimed result buffer stores a block of data from the operation unit is met by the buffer 248 of Dea (column 10, lines 53-56, and column 9, line 60- column 10, line 3); and

d) the claimed exclusive-OR unit performs an exclusive-OR operation between a block of data from the video input port and a block of data from the previous frame buffer is met by the description of difference calculator performs an X-OR function at column 6, lines 52-58 of Abramatic et al., whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video blocks.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea ' 208 and So '559 (New) in view of Yan '374.

Considering claim 9, the system of Dea and So discloses all the claimed limitation except for the claimed wherein the apparatus comprises part of a video conferencing system .

Nonetheless Dea teaches a compressed video data is being generated and utilized from the disclosed compression/decompression accelerator 120 as described at column 4, line 17-22. Additionally, Yan teaches the generated compressed video signal that is commonly having the application in videophone, video conference and other audio-visual transmission over networks as described at column 3, lines 52-64.

The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the compressed video data scheme as part of a video conference system in order to facilitate the benefit of bandwidth conservation in video data transmission.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208 and So '559 (New) in view of Hardiman ' 223.

Considering claim 11, the system of Dea and So discloses all the claimed limitations except for the claimed color space conversion circuit coupled between the video input port and the video input buffer.

Hardiman discloses an invention which relates to compression coding of a video program. Hardiman discloses the claimed color space conversion circuit coupled between the video input port and the video input buffer is met by the subsampler and color space converter 80 ( column 3, lines 47-57, column 6, lines 55-64, and FIG. 2), where the described video data/bus and the subsample FIFO are considered as the video input port and buffer, respectively.

Hardiman discloses that by implementing the color space conversion on video data provides the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57).

The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Dea and So by using the color space conversion circuit as taught by Hardiman for the stated benefit.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea, So and Abramatic et al. as applied to claim 13 above, and further in view of Yan '374.

Considering claim 18, the system of Dea, So and Abramatic et al. discloses all the claimed limitations except for the claimed wherein the apparatus comprises part of a video conferencing system .

Nonetheless Dea teaches a compressed video data is being generated and utilized from the disclosed compression/decompression accelerator 120 as described at column 4, line 17-22. Additionally Yan teaches the generated compressed video signal that is commonly having the application in videophone, video conference and other audio-visual transmission over networks as described at column 3, lines 52-64.

The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the compressed video data scheme as part of a video conference system in order to facilitate the benefit of bandwidth conservation in video data transmission.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea, So and Abramatic et al. as applied to claim 13 above, and further in view of Hardiman ' 223.

Considering claim 19, the system of Dea, So and Abramatic et al. discloses all the claimed limitations except for the claimed **color space conversion circuit** coupled between the video input port and the video input buffer.

Hardiman discloses an invention which relates to compression coding of a video program. Hardiman discloses the claimed color space conversion circuit coupled between the video input port and the video input buffer is met by the subsampler and color space converter 80 ( column 3, lines 47-57, column 6, lines 55-64, and FIG. 2), where the described video data/bus and the subsample FIFO are considered as the video input port and buffer, respectively.

Hardiman discloses that by implementing the color space conversion on video data provides the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57).

The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Dea, So and Abramatic et al. by using the color space conversion circuit as taught by Hardiman for the stated benefit.

***Response to Arguments***

9. Applicant's arguments with respect to claims 1, 13, 20 have been considered but are moot in view of the new ground(s) of rejection.

After further consideration and search , it is considered the reference of Dea in combination with So, new found reference, is applicable to the argued and amended limitations. Thus a new ground of rejection is presented and please see the above new ground of rejection .

***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Copy of Original filed paper***

11. The papers filed on ***August 26,2002*** (certificate of mailing dated ***August 20, 2002)*** have not been made part of the permanent records of the United States Patent and Trademark Office (Office) for this application (37 CFR 1.52(a)) because of damage from the United States Postal Service irradiation process. The above-identified papers, however, were not so damaged as to preclude the USPTO from making a legible copy of such papers. Therefore, the Office has made a copy of these papers, substituted them for the originals in the file, and stamped that copy:

COPY OF PAPERS

ORIGINALLY FILED

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If applicant wants to review the accuracy of the Office's copy of such papers, applicant may either inspect the application (37 CFR 1.14(d)) or may request a copy of the Office's records of such papers (*i.e.*, a copy of the copy made by the Office) from the Office of Public Records for the fee specified in 37 CFR 1.19(b)(4). Please do **not** call the Technology Center's Customer Service Center to inquiry about the completeness or accuracy of Office's copy of the above-identified papers, as the Technology Center's Customer Service Center will **not** be able to provide this service.

If applicant does not consider the Office's copy of such papers to be accurate, applicant must provide a copy of the above-identified papers (except for any U.S. or foreign patent documents submitted with the above-identified papers) with a statement that such copy is a complete and accurate copy of the originally submitted documents. If applicant provides such a copy of the above-identified papers and statement within **THREE MONTHS** of the mail date of this Office action, the Office will add the original mailroom date and use the copy provided by applicant as the permanent Office record of the above-identified papers in place of the copy made by the Office. Otherwise, the Office's copy will be used as the permanent Office record of the above-identified papers (*i.e.*, the Office will use the copy of the above-identified papers made by the Office for examination and all other purposes). This three-month period is not extendable.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linus H. Lo whose telephone number is (703) 305-4039.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller, can be reached at (703) 305-4795.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

lhl

November 12, 2002

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600